

## 1. Description

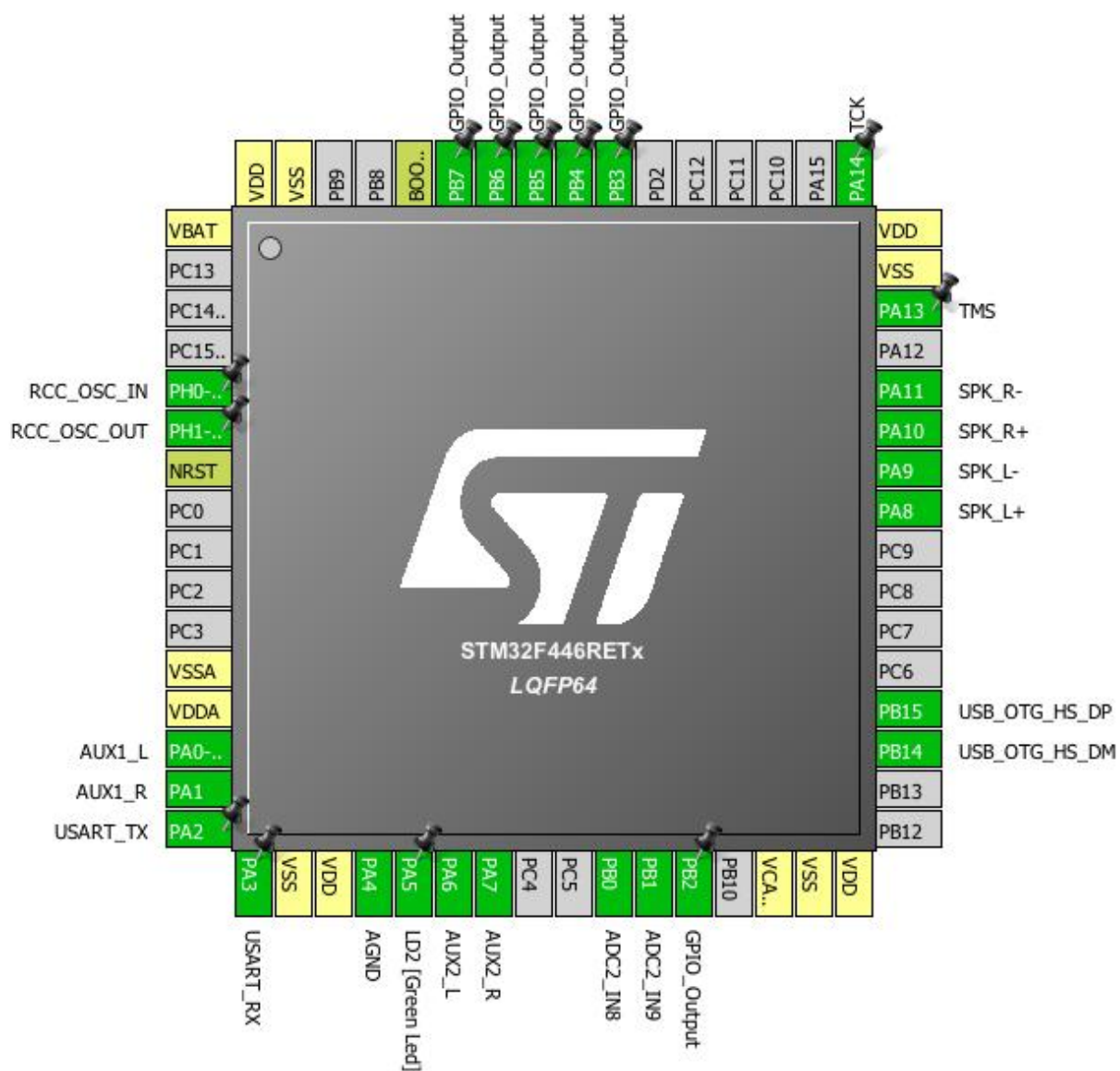
### 1.1. Project

Project Name	BTSP01
Board Name	NUCLEO-F446RE
Generated with:	STM32CubeMX 4.20.1
Date	01/24/2018

### 1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

## 2. Pinout Configuration



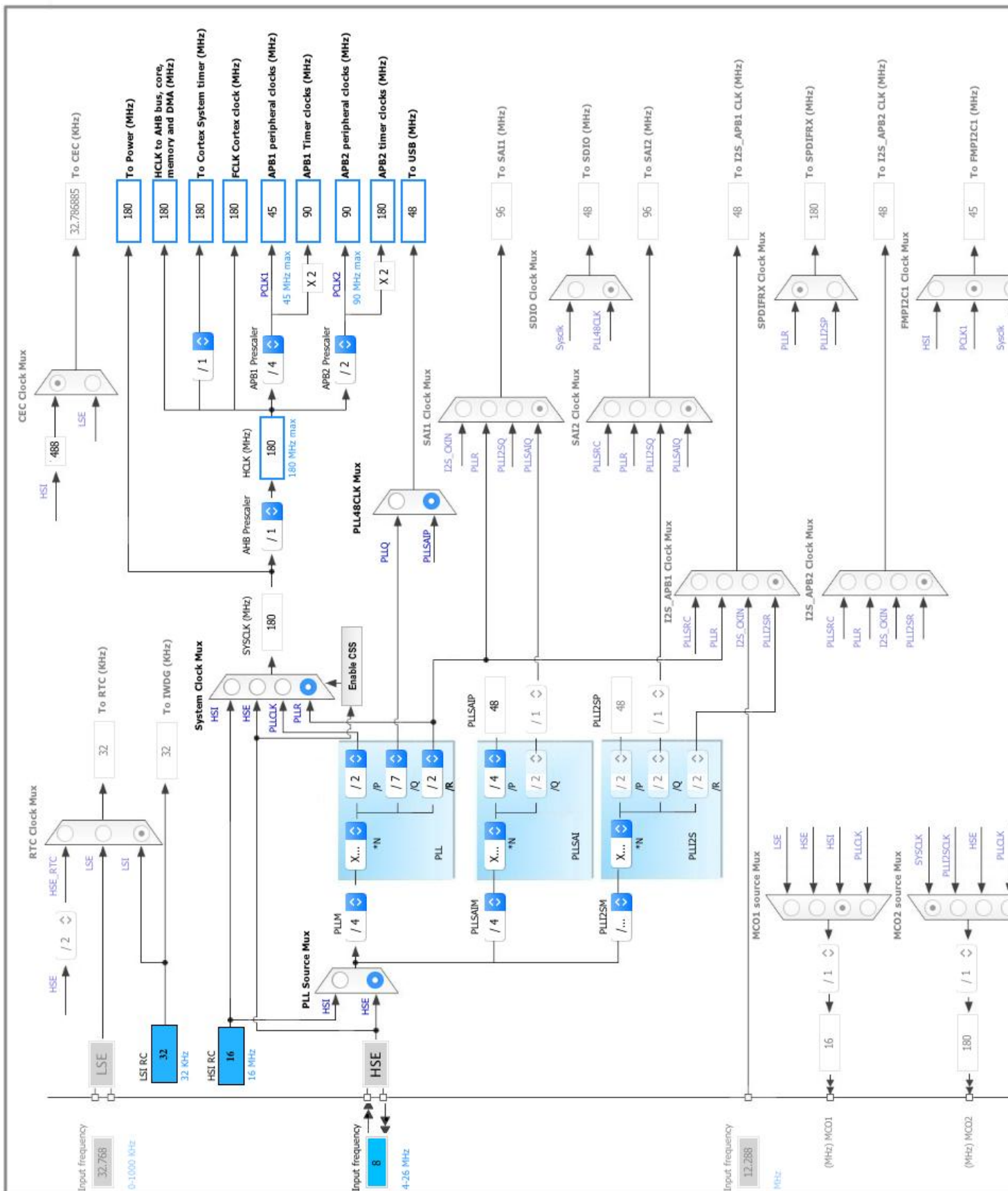
### 3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	ADC1_IN0	AUX1_L
15	PA1	I/O	ADC1_IN1	AUX1_R
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN4	AGND
21	PA5 *	I/O	GPIO_Output	LD2 [Green Led]
22	PA6	I/O	ADC1_IN6	AUX2_L
23	PA7	I/O	ADC1_IN7	AUX2_R
26	PB0	I/O	ADC2_IN8	
27	PB1	I/O	ADC2_IN9	
28	PB2 *	I/O	GPIO_Output	
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
35	PB14	I/O	USB_OTG_HS_DM	
36	PB15	I/O	USB_OTG_HS_DP	
41	PA8	I/O	TIM1_CH1	SPK_L+
42	PA9	I/O	TIM1_CH2	SPK_L-
43	PA10	I/O	TIM1_CH3	SPK_R+
44	PA11	I/O	TIM1_CH4	SPK_R-
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 *	I/O	GPIO_Output	
56	PB4 *	I/O	GPIO_Output	
57	PB5 *	I/O	GPIO_Output	
58	PB6 *	I/O	GPIO_Output	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
59	PB7 *	I/O	GPIO_Output	
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. IPs and Middleware Configuration

### 5.1. ADC1

mode: IN0

mode: IN1

mode: IN4

mode: IN6

mode: IN7

#### 5.1.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode **Enabled \***

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests **Enabled \***

End Of Conversion Selection **EOC flag at the end of all conversions \***

##### ADC\_Regular\_ConversionMode:

Number Of Conversion **5 \***

External Trigger Conversion Source **Timer 3 Trigger Out event \***

External Trigger Conversion Edge Trigger detection on the rising edge

Rank 1

Channel Channel 0

Sampling Time **28 Cycles \***

Rank **2 \***

Channel **Channel 1 \***

Sampling Time **28 Cycles \***

Rank **3 \***

Channel **Channel 4 \***

Sampling Time **28 Cycles \***

Rank **4 \***

Channel	<b>Channel 6 *</b>
Sampling Time	<b>28 Cycles *</b>
<u>Rank</u>	<b>5 *</b>
Channel	<b>Channel 7 *</b>
Sampling Time	<b>28 Cycles *</b>
<b>ADC_Injected_ConversionMode:</b>	
Number Of Conversions	0
<b>WatchDog:</b>	
Enable Analog WatchDog Mode	false

## 5.2. ADC2

**mode: IN8**

**mode: IN9**

### 5.2.1. Parameter Settings:

#### ADCs\_Common\_Settings:

Mode	Independent mode
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#### ADC\_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

#### ADC\_Regular\_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
<u>Rank</u>	1
Channel	Channel 8
Sampling Time	3 Cycles

#### ADC\_Injected\_ConversionMode:

Number Of Conversions	0
<b>WatchDog:</b>	
Enable Analog WatchDog Mode	false

### 5.3. RCC

#### High Speed Clock (HSE): Crystal/Ceramic Resonator

##### 5.3.1. Parameter Settings:

###### System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

###### RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

###### Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

### 5.4. SYS

#### Debug: Serial Wire

#### Timebase Source: SysTick

### 5.5. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

##### 5.5.1. Parameter Settings:

###### Counter Settings:



Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>2040 *</b>
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	<b>1 *</b>

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

#### Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

#### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

#### PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

#### PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

#### PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

## 5.6. TIM3

**Clock Source : Internal Clock**

### 5.6.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>2040 *</b>
Internal Clock Division (CKD)	No Division

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	<b>Update Event *</b>

## 5.7. TIM7

**mode: Activated**

### 5.7.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>8999 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>10000 *</b>

#### Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
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## 5.8. USART2

**Mode: Asynchronous**

### 5.8.1. Parameter Settings:

#### Basic Parameters:

Baud Rate	<b>9600 *</b>
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 5.9. USB\_OTG\_HS

### Internal FS Phy: Host\_Only

#### 5.9.1. Parameter Settings:

Speed	Host Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Physical interface	Internal Phy
Signal start of frame	Disabled

## 5.10. USB\_HOST

### Class For HS IP: Audio Host Class

#### 5.10.1. Parameter Settings:

**Host Configuration:**

USBH_MAX_NUM_ENDPOINTS (Maximum number of endpoints)	<b>4 *</b>
USBH_MAX_NUM_INTERFACES (Maximum number of interfaces)	10
USBH_MAX_NUM_SUPPORTED_CLASS (Maximum number of supported class)	<b>2 *</b>
USBH_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBH_KEEP_CFG_DESCRIPTOR (Keep the configuration into RAM)	Enabled
USBH_MAX_SIZE_CONFIGURATION (Maximum size in bytes for the Configuration Descriptor)	256
USBH_MAX_DATA_BUFFER (Maximum size of temporary data)	512
USBH_DEBUG_LEVEL (USBH Debug Level)	0: No debug message

**CMSIS\_RTOS:**

USBH_USE_OS (Enable the support of an RTOS)	Disabled
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\* User modified value

## 6. System Configuration

### 6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	AUX1_L
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	AUX1_R
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	AGND
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	AUX2_L
	PA7	ADC1_IN7	Analog mode	No pull-up and no pull-down	n/a	AUX2_R
ADC2	PB0	ADC2_IN8	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC2_IN9	Analog mode	No pull-up and no pull-down	n/a	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	SPK_L+
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	SPK_L-
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	SPK_R+
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	SPK_R-
USART2	PA2	USART2_TX	Alternate Function Push Pull	Pull-up	Very High *	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	Very High *	USART_RX
USB_OTG_HS	PB14	USB_OTG_HS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB15	USB_OTG_HS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

## 6.2. DMA configuration

DMA request	Stream	Direction	Priority
TIM1_UP	DMA2_Stream5	Memory To Peripheral	<b>Very High *</b>
ADC1	DMA2_Stream0	Peripheral To Memory	<b>Medium *</b>

### TIM1\_UP: DMA2\_Stream5 DMA request Settings:

Mode: **Circular \***  
 Use fifo: **Enable \***  
 FIFO Threshold: Full  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Half Word  
 Memory Data Width: Half Word  
 Peripheral Burst Size: Single  
 Memory Burst Size: Single

### ADC1: DMA2\_Stream0 DMA request Settings:

Mode: **Circular \***  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Half Word  
 Memory Data Width: Half Word

### 6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM7 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream5 global interrupt	true	0	0
USB On The Go HS global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
USART2 global interrupt	unused		
USB On The Go HS End Point 1 Out global interrupt	unused		
USB On The Go HS End Point 1 In global interrupt	unused		
FPU global interrupt	unused		

\* User modified value



## ***7. Power Consumption Calculator report***

### 7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	027107_Rev5

### 7.2. Parameter Selection

Temperature	25
Vdd	null

## 8. Software Project

### 8.1. Project Settings

Name	Value
Project Name	BTSP01
Project Folder	/Users/togashitoyohiko/Documents/OpenSTM32/BTSP01
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F4 V1.16.0

### 8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No