

1. Description

1.1. Project

Project Name	BTSP01
Board Name	NUCLEO-F446RE
Generated with:	STM32CubeMX 4.20.1
Date	02/17/2019

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

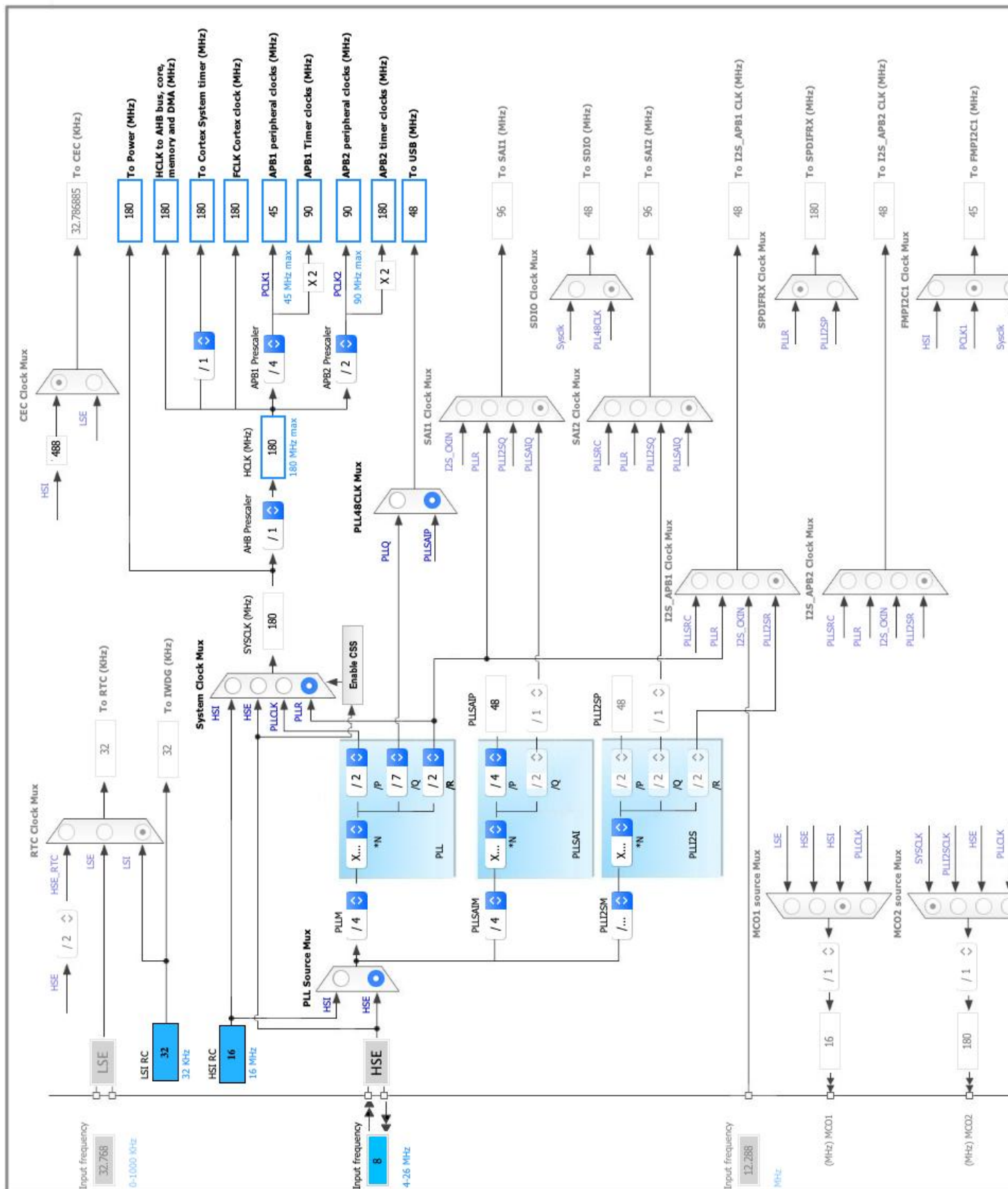
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Output	LCM-DB13
3	PC14-OSC32_IN *	I/O	GPIO_Output	LCM-DB14
4	PC15-OSC32_OUT *	I/O	GPIO_Output	LCM-DB15
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Output	LCM-DB0
9	PC1 *	I/O	GPIO_Output	LCM-DB1
10	PC2 *	I/O	GPIO_Output	LCM-DB2
11	PC3 *	I/O	GPIO_Output	LCM-DB3
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	ADC1_IN0	AUX1_L
15	PA1	I/O	ADC1_IN1	AUX1_R
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN4	AGND
21	PA5 *	I/O	GPIO_Output	LD2 [Green Led]
22	PA6	I/O	ADC1_IN6	AUX2_L
23	PA7	I/O	ADC1_IN7	AUX2_R
24	PC4 *	I/O	GPIO_Output	LCM-DB4
25	PC5 *	I/O	GPIO_Output	LCM-DB5
26	PB0	I/O	ADC2_IN8	LCM-YN
27	PB1	I/O	ADC2_IN9	LCM-XN
28	PB2 *	I/O	GPIO_Output	LCM-YP
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
35	PB14	I/O	USB_OTG_HS_DM	
36	PB15	I/O	USB_OTG_HS_DP	
37	PC6 *	I/O	GPIO_Output	LCM-DB6
38	PC7 *	I/O	GPIO_Output	LCM-DB7
39	PC8 *	I/O	GPIO_Output	LCM-DB8

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
40	PC9 *	I/O	GPIO_Output	LCM-DB9
41	PA8	I/O	TIM1_CH1	SPK_L+
42	PA9	I/O	TIM1_CH2	SPK_L-
43	PA10	I/O	TIM1_CH3	SPK_R+
44	PA11	I/O	TIM1_CH4	SPK_R-
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
51	PC10 *	I/O	GPIO_Output	LCM-DB10
52	PC11 *	I/O	GPIO_Output	LCM-DB11
53	PC12 *	I/O	GPIO_Output	LCM-DB12
55	PB3 *	I/O	GPIO_Output	LCM-XP
56	PB4 *	I/O	GPIO_Output	LCM-CS
57	PB5 *	I/O	GPIO_Output	LCM-RS
58	PB6 *	I/O	GPIO_Output	LCM-WR
59	PB7 *	I/O	GPIO_Output	LCM-RD
60	BOOT0	Boot		
61	PB8 *	I/O	GPIO_Output	LCM-BL
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0

mode: IN1

mode: IN4

mode: IN6

mode: IN7

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode **Enabled ***

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests **Enabled ***

End Of Conversion Selection **EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion **5 ***

External Trigger Conversion Source **Timer 3 Trigger Out event ***

External Trigger Conversion Edge Trigger detection on the rising edge

Rank 1

Channel Channel 0

Sampling Time **28 Cycles ***

Rank **2 ***

Channel **Channel 1 ***

Sampling Time **28 Cycles ***

Rank **3 ***

Channel **Channel 4 ***

Sampling Time **28 Cycles ***

Rank **4 ***

Channel	Channel 6 *
Sampling Time	28 Cycles *
<u>Rank</u>	5 *
Channel	Channel 7 *
Sampling Time	28 Cycles *
ADC_Injected_ConversionMode:	
Number Of Conversions	0
WatchDog:	
Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN8

mode: IN9

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode
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ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
<u>Rank</u>	1
Channel	Channel 8
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0
WatchDog:	
Enable Analog WatchDog Mode	false

5.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

5.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.5. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	4081 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	2040 *
Fast Mode	Disable
CH Polarity	Low *
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	2040 *
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	2040 *
Fast Mode	Disable
CH Polarity	Low *
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	2040 *
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.6. TIM3

Clock Source : Internal Clock

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	2040 *
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Update Event *

5.7. TIM7

mode: Activated

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	8999 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	10000 *

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
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5.8. USART2

Mode: Asynchronous

5.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	9600 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.9. USB_OTG_HS

Internal FS Phy: Host_Only

5.9.1. Parameter Settings:

Speed	Host Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Physical interface	Internal Phy
Signal start of frame	Disabled

5.10. USB_HOST

Class For HS IP: Audio Host Class

5.10.1. Parameter Settings:

Host Configuration:

USBH_MAX_NUM_ENDPOINTS (Maximum number of endpoints)	4 *
USBH_MAX_NUM_INTERFACES (Maximum number of interfaces)	10
USBH_MAX_NUM_SUPPORTED_CLASS (Maximum number of supported class)	2 *
USBH_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBH_KEEP_CFG_DESCRIPTOR (Keep the configuration into RAM)	Enabled
USBH_MAX_SIZE_CONFIGURATION (Maximum size in bytes for the Configuration Descriptor)	256
USBH_MAX_DATA_BUFFER (Maximum size of temporary data)	512
USBH_DEBUG_LEVEL (USBH Debug Level)	0: No debug message

CMSIS_RTOS:

USBH_USE_OS (Enable the support of an RTOS)	Disabled
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* User modified value

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	AUX1_L
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	AUX1_R
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	AGND
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	AUX2_L
	PA7	ADC1_IN7	Analog mode	No pull-up and no pull-down	n/a	AUX2_R
ADC2	PB0	ADC2_IN8	Analog mode	No pull-up and no pull-down	n/a	LCM-YN
	PB1	ADC2_IN9	Analog mode	No pull-up and no pull-down	n/a	LCM-XN
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	SPK_L+
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	SPK_L-
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	SPK_R+
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	SPK_R-
USART2	PA2	USART2_TX	Alternate Function Push Pull	Pull-up	Very High *	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	Very High *	USART_RX
USB_OTG_HS	PB14	USB_OTG_HS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB15	USB_OTG_HS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB13
	PC14-	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB14

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	OSC32_IN					
	PC15-OSC32_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB15
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB0
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB1
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB2
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB3
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB4
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB5
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-YP
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB6
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB7
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB8
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB9
	PC10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB10
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB11
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-DB12
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-XP
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-CS
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-RS
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-WR
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-RD
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCM-BL

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Medium *
TIM1_UP	DMA2_Stream5	Memory To Peripheral	Very High *

ADC1: DMA2_Stream0 DMA request Settings:

Mode: **Circular ***
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Half Word
 Memory Data Width: Half Word

TIM1_UP: DMA2_Stream5 DMA request Settings:

Mode: **Circular ***
 Use fifo: **Enable ***
 FIFO Threshold: Full
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Half Word
 Memory Data Width: Half Word
 Peripheral Burst Size: Single
 Memory Burst Size: Single

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM7 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream5 global interrupt	true	0	0
USB On The Go HS global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
USART2 global interrupt	unused		
USB On The Go HS End Point 1 Out global interrupt	unused		
USB On The Go HS End Point 1 In global interrupt	unused		
FPU global interrupt	unused		

* User modified value

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	027107_Rev5

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	BTSP01
Project Folder	/Users/togashitoyohiko/Documents/OpenSTM32/BTSP01
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F4 V1.16.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No